

ABSTRACT

The present invention provides a receiver including:
A/D converters (1-1 to 1-4) for converting receiving analog
signals (I1, Q1, I2, Q2) into digital signals; a quantizing
5 error reduction signal generator (2) for generating a random
noise quantizing error reduction; adders (3-1 to 3-4) for
adding the converted digital signal and the quantizing error
reduction signal; bit shift circuits (4-1 to 4-4) for
reducing a bit number of addition; low-pass filters (5-1,
10 5-2) for removing a quantizing error reduction signal
included in the digital signal having a reduced bit number;
matched filters (6-1, 6-2); and a demodulation section (7).

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